ABSTRACT

The invention relates to a dual masked spacer etch for improved dark current performance in imagers. After deposition of spacer material such as oxide, N-channel regions are first opened for N^+ source/drain implant and P-channel regions are then opened for P^+ source/drain implant. Prior to the N^+ source/drain implant, the wafer receives a patterned first spacer etch. During this first spacer etch, the photosensor region is covered with resist. Prior to the P^+ source/drain implant, a masked second spacer etch is performed. Again the photosensor region is protected with photoresist. In such a manner, spacers are formed on the gates of both the N-channel and P-channel transistors but in the photodiode region the spacer insulator remains.